OS iProject Three

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Round Robin scheduling with a Quantum of two (2) cycles
Project 3

> load

CPU

MA

Ready Queue

A9 A9 A2 01 EC 13 00 AC
0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00
Project 3

> load
pid 0 loaded in seg 0
>

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

new PCB()
MMU assigns segment 0, sets base and limit

Ready Queue

CPU

MA

0 1 2

A9 A9 A2 01 EC 13 00 AC
0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00
> load
pid 0 loaded in seg 0
> load

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

Ready Queue

CPU

MA

A9 A9 A2 01 EC 13 00 AC
0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00
> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
>
PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

new PCB()
MMU assigns segment 1, sets base and limit

Ready Queue
> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

Ready Queue

CPU

A9 A9 A2 01 EC 13 00 AC
0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00

MA

0

1

2

iProject 3
> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
>
new PCB()
MMU assigns
segment 2, sets
base and limit
Project 3

> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

CPU

MA

0
1
2

A9 A9 A2 01 EC 13 00 AC
0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00
$>$ load
pid 0 loaded in seg 0
$>$ load
pid 1 loaded in seg 1
$>$ load
pid 2 loaded in seg 2
$>$ runall

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

Context Switch

A9 A9 A2 01 EC 13 00 AC
0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00
> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

Context Switch

A9 A9 A2 01 EC 13 00 AC
0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00
> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

CPU cycle

A9 A9 A2 01 EC 13 00 AC
0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00
> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

CPU cycle
Project 3

> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Context Switch

Ready Queue

> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

CPU

MA

A9 A9 A2 01 EC 13 00 AC
0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00
iProject 3

> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

Context Switch

MA

CPU

A9 A9 A2 01 EC 13 00 AC
0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00
> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

Context Switch

> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall
iProject 3

> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

Ready Queue

CPU cycle

A9 A9 A2 01 EC 13 00 AC
0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00
> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

CPU cycle

A9 A9 A2 01 EC 13 00 AC
0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00
Project 3

> load
pid 0 loaded in seg 0
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pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Context Switch

Ready Queue

> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

MA

CPU

0

1

2

A9 A9 A2 01 EC 13 00 AC 0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01 EC 13 00 AC 0B 00 8D 00
iProject 3

> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

Context Switch

> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

CPU

MA

0

1

2
Project 3

> load
 pid 0 loaded in seg 0
> load
 pid 1 loaded in seg 1
> load
 pid 2 loaded in seg 2
> runall

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

Context Switch

A9 A9 A2 01 EC 13 00 AC
0B 00 8D 00 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00
> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

CPU cycle

> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall
> load
  pid 0 loaded in seg 0
> load
  pid 1 loaded in seg 1
> load
  pid 2 loaded in seg 2
> runall

PCB for pid 0
  Mem segment: 0
  PC, AC, X, Y, Z
  Base, Limit

PCB for pid 1
  Mem segment: 1
  PC, AC, X, Y, Z
  Base, Limit

PCB for pid 2
  Mem segment: 2
  PC, AC, X, Y, Z
  Base, Limit

CPU cycle
iProject 3

> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

Ready Queue

Context Switch

> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
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pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
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pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
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pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
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pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
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pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

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pid 0 loaded in seg 0
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pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
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pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch

Load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

Context Switch
iProject 3

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> load
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PCB for pid 1
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Base, Limit

PCB for pid 2
Mem segment: 2
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PCB for pid 1
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PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

Context Switch
iProject 3

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PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

Context Switch

> load
pid 0 loaded in seg 0
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pid 2 loaded in seg 2
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PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

CPU

MA

Ready Queue

Context Switch

A9 A9 A2 01 EC 13 00 AC
0B 00 8D F0 00 EE 0B 00
D0 F5 00 00 A9 A9 A2 01
EC 13 00 AC 0B 00 8D 00
> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

CPU cycle
```
> load
pid 0 loaded in seg 0
> load
pid 1 loaded in seg 1
> load
pid 2 loaded in seg 2
> runall

PCB for pid 0
Mem segment: 0
PC, AC, X, Y, Z
Base, Limit

PCB for pid 1
Mem segment: 1
PC, AC, X, Y, Z
Base, Limit

PCB for pid 2
Mem segment: 2
PC, AC, X, Y, Z
Base, Limit

Ready Queue

CPU cycle
```
Context Switch

... and so on, until the processes are complete.